1K/2K Select

The 2114 and 2716 are very popular and inexpensive RAMs and EPROMs, and this is the reason they were chosen for the RRM-14 board. However, this does raise some difficulties in the design of address decoders, particularly if the use of the board is to be restricted as little as possible. This difficulty is caused by the mutual incompatibility of a 1K select on the one hand, and a 2K select on the other.

Reference to the circuit diagram will show that 74LS139 address decoders have been adopted to provide a mixture of 1K and 2K selects, for the RAMs and ROMs respectively. Some are dedicated to 1K use, some to 2K, and one section can be either 1K or 2K according to how a link is made.

4K Select

As the chosen 4K pages may be anywhere in the memory map, all sixteen pages must be independently available, and the most suitable device to provide this is a type 74LS154.

General

The RRM-14 board is high quality, and uses plated through holes. It is likely that it will be reconfigured by the user again and again, as his plans and experiments change. There is thus a dilemma which has been faced by the designers of this board - it will be used as a "breadboard" in many applications, but unlike a breadboard, it is too expensive to throw away once a particular experiment or application is over.

The main "wear" on a board occurs when tracks are cut and re-joined again and again - eventually they lift and fall off. On this board most of the areas where track cutting would have been carried out by the user are already separate, e.g. spare inputs of gates etc. are isolated for experimental use. It is suggested that connections be made by wire wrapping on special 0.1" pitch pin assemblies fitted in suitable places on the board.

It is accepted that it is tedious for the user to make connections in this manner which could easily be pre-connected in the copper track itself, but this is a small price to pay for the greatly extended life the board will have if track cutting and re-joining by soldering is not necessary.

(There is one exception to this, and that is the method of using the board in 16-bit data bus systems. It is hardly likely that someone will be changing the board from an 8-bit to a 16-bit bus on a regular basis, and so the track has been hard wired to the "normal" 8-bit bus arrangement.)

For truly experimental use there is no need even to wire wrap the links - miniature push fit wire, or proprietary hooks (e.g. "E-Z Hooks") can be used for temporary purposes, for example to run a

RAM

The 2114 devices are 1K x 4 (bit), and are invariably used in pairs to make a 1K x 8 (bit) RAM, described throughout the remainder of this document simply as "1K". (By the way, the term 1K (big K) needs defining - this is 2^{10} = 1024, unlike 1k (little k) which means 10^3 = 1000).

As there are twelve 2114 devices there are therefore six pairs. Each pair shares the same "chip select" and the six chip selects are called RAM0, RAM1, RAM2, RAM 3, RAM4, and RAM5.

ROM

The ROM devices (usually EPROMs type 2716) are each 2K x 8 (bit), or "2K" for short. There are four ROMs and the four "output enables" (which are used like the chip selects of the RAMs) are called ROM0, ROM1, ROM2, and ROM3.

Addressing

Ultimate flexibility would have all these lines individually locatable anywhere in the memory space, but as the board is already quite complex enough, the following restrictions have been accepted:-

(i) The RAMs and ROMs can be located only at 1K/2K/4K boundaries (i.e. RAM can start at 0000h, 0400h, 0800h, etc. but not between).

(ii) 4K of continuous RAM is assumed to be required on just one 4K "page" - not "dotted about" the memory map.

(iii) 4K of continous ROM is assumed similarly to be located on just one 4K page.

(Note that although not all the RAM or ROM described above need be fitted, the data bus buffer will however be enabled for the whole of the page, whether or not the RAMs or ROMs are actually plugged in.)

The 4K of RAM on the single 4K RAM page is RAM0, 1, 2, 3.
" " " ROM " " " " ROM " " ROM0, 1.

This leaves 2K of RAM (RAM4, 5), and 4K of ROM (ROM2, 3). The buffer is enabled directly by these two pairs of signals, and so the very much (in the past) desired result is achieved: namely the ability to have RAM and ROM mixed on the same page. When these memory devices (RAM4, 5, and ROM2, 3) are selected their select lines also enable the buffer, when they are not selected they do not enable the buffer.

program in RAM at its "target" address prior to committing it to an EPROM.

Of course the owner of the board is entitled to use it in any way he wants, and if he does not have the enthusiasm or facilities for wire-wrapping he may of course make the links with soldered connections. Generous 1.0 mm holes have been used to minimise the risk of damaging the through-hole plating when soldering and de-soldering.

Care has also been taken in the layout to make sure that vulnerable connections which run between the legs of I.C.s etc., are routed for preference on the visible side of the board rather than buried say underneath an I.C. socket.

Applications

It is not really very easy to suggest specific applications as there is not intrinsically not much a memory card can do other than be a memory card!

However, there are some obvious applications, and some not so obvious, and they are listed as follows:-

1. Small ("starter") system memory card - the one card can serve the need for both ROM and RAM. Unlike the dynamic RAM card (only available to Z80(A) users), which can provide no smaller memory than 16K blocks, the RAM can be built up on this board 1K at a time starting with as little as just two 2114 chips.

2. 5V only system. One great disadvantage of the very inexpensive 4116 dynamic RAMs is their need for +12V and -5V power rails in addition to the normal +5V, so an alternative RAM of some sort is needed when only a single +5V supply is in use.

3. Mixed RAM and ROM on the same 4K page. The RRM-14 is designed to permit the use of software which has this requirement, and which cannot be run on conventional memory boards without the need for re-wiring, track-cutting etc.

4. "Mopping up" spare memory cards and spare memory devices. Many users will have old memory cards (e.g. Kemitron MXA-1 2K RAM card) which have now been superceded by new developments (e.g. 16K RAM). Rather than throw away the "obsolete" cards, they can be pressed into service, and the RRM-14 card can be used to plug any uneven "gaps" which result. Many users will have built up a store of surplus 2114 memory chips, and they can be usefully employed on the RRM-14 card. For example the RRM-14 can be purchased primarily as an EPROM card - the fact that it can accept some old 2114 memories as will can be looked on as a most welcome bonus.

5. Experimental use. There are times when the option of RAM or ROM at exactly the same address is needed. For example, most of the time a BASIC interpreter will require RAM in its text area, but the option of a program burned into an EPROM, which can be run at

the same address, can prove useful - e.g. a disassembler program may be instantly required without waiting for it to be loaded from tape. (The NIBL BASIC for the old fashioned SC/MP microprocessor was ideal for this application - it had six distinct "pages" which could have different programs in RAM or ROM.)

The select signals for the RAM and ROM on the RRM-14 card are readily available, and can be routed through a front-panel switch. Provided a program is not actually being executed in the devices when the switch is thrown, the RAM and ROM devices can be interchanged without the need to turn off the power, simply by operating the switch.

6. Generous "patch" areas have been provided, and these can be used in a variety of different applications:

7. Evaluating new devices. As new memory devices are introduced they can be tried out on the patch areas - they are bound to use many of the signals already on the board (read, write, address, data, etc.). If a small battery is used with a CMOS RAM, such as the 2K 6116, a non-volatile store can be constructted - much of the benefit of an EPROM programmer, without the expense.

8. As a controller. A few 8-bit output latches can be fitted to switch lamps and relays etc. on and off and so avoid the need for a separate card. The latches could be memory-mapped or the spare half of the 74LS139 could be adopted in conjunction with the bus NIOREQ line to give I/O mapping.

9. As a stand alone CPU. This is a fanciful idea but quite possible. There are times when a microprocessor can be employed to do a simple job, e.g. turning a few controls on and off in sequence, monitor a burglar alarm, etc. In such an application the CPU and crystal etc. can be mounted on the patch area with a certain amount of I/O, and the RRM-14 board array will provide as little or as much memory as is needed.

10. Although consideration has not been given to the following application it seems reasonably possible that the RRM-14 card could be used with some alternative 24-pin memory devices instead of the normal 2716 2K EPROM. Some alteration to certain lines would certainly be needed, and may or may not be practical.

The reason for these comments is based on the following observations:-

As the card is designed as a ROM/RAM card, there is a bi-directional data bus transceiver already provided. This makes it much easier to substitute RAM chips for ROM chips.

The chip selects ROM2 and ROM3 are not preconnected; they could easily be taken directly to the 4K select outputs of the 74LS154, so that 4K devices could be used in at least two of the 24-pin sockets (but note other connections would need altering as well).

ADDRESS DECODING

Page Selects PS0 to PSF

These are the 16 outputs from U5 (74LS154). Each output gives a 4K "page select" signal.

Page Select U (PS'U')

This input (to connection pin 9) selects ROM0 and ROM1, which together fill a whole 4K page.

Page Select V (PS'V')

This input (to connection pin 10) selects a "ROM/RAM" page. ROM can be selected either in the first half of the 4K page, or in the last half, or indeed in both halves. (It would of course not then be a "ROM/RAM" page any longer.)

Join pins 26-28 for ROM in the first 2K (ROM2)
or Pins 27-29 for ROM in the last 2K (ROM3)
(or both to fill the whole page with ROM).

(There are two connection pins (10 and 11) provided for page select V, this is for use when ROM and RAM is being mixed on the same page - the duplicate pin can be used to take the 4K page select to the RAM address decoder, to save putting two wires on the same pin.)

Page Select W (PS'W')

This input (to connection pin 15) selects RAM0, 1, 2, 3, which together make up a whole 4K page.

Page Select X (PS'X')

This input (to connection pin 35) is used to select either, or both, RAM4 and RAM5 (4 chips in all).

If for example, PSV has already been used as described earlier for a ROM/RAM page, then PS'X' can be made the same as PS'V' (by connecting pins 11 and 35). If this is done then one or both of RAM4 and 5 can be fitted into a suitable empty space on the selected 4K page:-

Join pins 37-41/36-40 for RAM in the first 2K
Join pins 39-41/38-40 for RAM in the last 2K.

It is allowable to leave the combined page (PSV and PSX) partially empty - for example 2K of ROM, then 1K of empty space and finally 1K of RAM, the spare 1K of RAM being released for use elsewhere.

Page Select Y (PS'Y')

This input (to connection pin 1) is used for "mopping up" any surplus ROM or RAM, which has been displaced from other pages. The RAM requires a 1K select, and the ROM requires 2K:-

For 1K link connection pins 7-8
For 2K link connection pins 7-6

If 1K has been selected then the 4K page will be divided into four 1K blocks, which will be the four outputs (pins 2, 3, 4, 5) in order first to last, and the appropriate one can be joined to RAM4 (connection pin 40), or RAM5 (connection pin 41), whichever is unused at this stage.

Page Select Z (PS'Z')

If there is any ROM or RAM unallocated after the five pages U, V, W, X, Y, have been dealt with, the spare memory can be located on page Z. There is no specific pin for Page Select Z as any of the unused outputs of U5 (74LS154) will serve this purpose, and should be connected to whichever memory is "spare" (one of ROM 2, 3, or RAM 4, 5.

Note that the addressing for the memory in this case is partially decoded, i.e. the whole of the 4K page will be devoted to the 1 or 2K of memory.

5.1 CONSTRUCTIONAL NOTES

1. Read all documents very carefully before starting.

2. There are no Static Sensitive devices in the present kit of parts, so everything may be handled without special precautions. The memory devices used will be sensitive to damage and must be handled appropriately. Identify all the components and using the Component Overlay, and the Parts List, work out where they all going to fit before soldering anything.

3. The "B" side of the board is the side which is visible when the card is viewed in the same way as is illustrated in the Component Overlay diagram, i.e. the diagram is drawn looking at the "B" side. The other side is the "A" side and the components are inserted from the "B" side and soldered on the "A" side, when the time comes. The number on the board carries an "A" or "B" suffix to help identify which side is which.

4. Carry out any drilling or filing necessary to fit the card in the rack, and to bolt on the front panel. (This work should not be necessary, but if it was it would be a lot more difficult once the card had been assembled.) In order to get the longest life from the edge connector sockets in the rack it is a good idea to chamfer lightly all of the edges of the card around the gold-plated area - but do not overdo this!

5. Check that there are no obvious defects on the board, e.g. damaged or short-circuited track etc. Look especially beneath the IC socket positions since they will be hidden in the finished job.

6. Consult the Component Overlay, and the Parts List, to determine what goes where. Any convenient order may be followed, but a typical method is to start with the lowest height components and work up.

   The following steps can be used as a check-list:

   (c) Fit IC sockets U1-U25. Be sure to use an acceptable type of socket if you are going to take advantage of the board supplier's fault-finding service - see the Fault Finding Section of this Manual for further remarks on this subject. Make the identifying mark on the socket correspond to the Pin 1 end of the IC. Do not plug any components into their sockets yet.

   (e) Fit C1-14. (Note! C14 is a polarised type which must be fitted the correct way round. The "+" lead of the capacitor will be marked "+", or can be identified by a process of elimination as being the lead which is not marked "-".) Consult the sketches in the right-hand column of the Parts List (at the back of this Manual) for further guidance. Go

through the whole list of capacitors, comparing the different types and quantities supplied, if you are not used to capacitor markings, until you are sure you know which is which.

(f) Fit the 0.1" pitch pin assemblies. These will usually be supplied ready for use according to the chart on the parts list, but if they are not, they can be cut to length with a sharp knife, and any posts which need removing can be carefully be pulled out with pliers. Do not solder all positions until you are sure that the assemblies are perfectly located and perpendicular to the board (for neatness' sake). Pass the short length of the pins thorough the card from the top and solder on the underside, like all the other components. (For very low-profile work they can be mounted upside down, i.e. the long ends through the card, and the surplus cut off after soldering.)

(g) Fit the 9-pin 0.1" socket strip which is used as the socket for SIL 1. The socket strip comprises a number of formed sockets on one-piece carriers. Do not break off the carriers yet! Solder the strips in position and when you are sure everything is correct, and only when, break off the carriers by bending them gently back and forth with long nosed pliers, being certain not to distort the socket parts in any way.

7. If you wish, use a suitable solvent to remove any flux deposits from the track side of the board. (Note! Some solvents also dissolve some types of plastic.) Also note that over-zealous use of flux-removing solvents can actually cause trouble, by washing impurities into connectors and IC sockets. You can give some protection by covering them with masking tape, but in many cases it is better to ignore this step altogether.

8. If desired the board may be laquered on the underside. A suitable printed circuit board laquer should be used, and similar precautions should be taken as described in the previous paragraph (no. 7), to prevent the connectors and IC sockets from becoming contaminated. It is probably safest to ignore this step if you are in any doubt, as a lot of damage can be done through lack of experience here. (Note! be sure not to laquer the gold-plated edge connector on the card.)

This concludes the constructional notes. The next section of the Manual covers testing and setting up.

SETTING UP

Connect the various pins according to the application. A detailed description of the addressing arrangements has already been given, but a chart ("RRM-14 General Guidance on Address Selection Links etc.") is also included with the circuit diagrams which summarises the requirements and lists a few specific examples. The RRM-14 card was designed at a time when the Z80A and large quantities of dynamic RAM were not so frequently seen, and most of the examples given on the chart have little or no relevance to the needs of a modern "Interak 1" system user.

In due course the chart will be revised, to give some examples which are more likely to be of interest to Interak 1 users, but if this has not been done by the time you receive these notes then you will have to take the examples as indicating the principles only rather than giving exact instructions.

TESTING

Testing is simply a matter of plugging in the card and seeing if it works - fault finding is a little more difficult.

Some points which may be helpful at this stage of the task are as follows:-

1. CPU operating frequency. No problems should be experienced with SC/MP, even at its full operating frequency 4 MHz, nor with the Z80-CPU at 2 MHz, if standard 450 ns (or faster) memories are used.

   Some closer investigation is needed if the Z80A-CPU is used at 4 MHz (which is the recommendation nowadays). Preliminary calculations reveal that much shorter access times are required in this case:

   Using the Z80A-CPU at 4 MHz with no wait states:

Memory Read/Write	300 ns
Op-code Fetch (Program Execution)	200 ns

   If a single wait state can be added, these can be increased to the following:

Memory Read/Write	550 ns
Op-code Fetch (Program Execution)	450 ns

   In an Interak 1 system there is on the LKP-1 card a circuit which can add wait states to chosen memory addresses, so the addition of wait states if necessary is very easy to implement. Users wishing to use the RRM-14 card outside an Interak 1 system must make their own arrangements. It is suggested that such users purchase a copy of the LKP-1 Manual, and build the circuit on a

patch area on the RRM-14 card.

2. The easiest parts of the decoding are for the 4K pages, since this is carried out within the 74LS154 integrated circuit without assistance from the user. There is more chance for error in the later stages, when splitting up pages, mixing ROM and RAM on the same page etc., so initial tests are best carried out with the simple decoding first if possible.

3. If the RRM-14 is being added to an existing system check it on some unused pages first. ROM is easiest because it is read only, then RAM should be tried to test more of the circuit (i.e. write as well as read). If the host system "crashes" when the RRM-14 card is added, try removing all the page selects (e.g. remove the 74LS154) to ensure there is no addressing conflict, then if trouble still persists remove the various buffers U22 to U25 to localise the fault. If the system still crashes with all the buffers removed, this suggests a short circuit somewhere on the edge connector on the card, or at least nearby.

4. If you have the facilities on your system, check the RRM-14 card in the following order:

   (i) Try reading ROMs at a chosen page.
   (ii) Try reading and writing RAMs at a chosen page.
   (iii) Try executing Op-codes in fast memory (usually the RAM).
   (iv) Try executing Op-codes in slow memory (usually the ROM).

   If you have a choice of CPU speeds e.g. 2 MHz and 4 MHz for a Z80A-CPU then try the slower speed first, and get good results before proceeding to 4 MHz.

5. An extender card can be purchased from your Interak supplier, which greatly aids setting up and testing new cards, but remember that at the high speeds the Interak 1 computer works, it is just possible that a card which is perfectly constructed and set up can still give poor results (corrupted bits etc.) when it is subject to the extra delays and noise induced by operating it on an extender card. From time to time during fault finding it is worth while plugging it directly into the rack to see that there really is still a fault present, and that it has not inadvertently been fixed.

6. System "noise" can cause poor performance. This problem if it exists has to be tackled as a separate subject, but to make sure that it is not responsible for any troubles which may be experienced on the RRM-14 card, it should be plugged in as closely as possible to the CPU card in the system rack.

This concludes the section on testing and setting up.

① THE FOLLOWING PINS ARE USUALLY LINKED IN EVERY CASE:
13-34/17-18/24-33/25-32/30-31. OTHER LINKS ARE MADE ACCORDING TO SPECIFIC REQUIREMENTS.

② EXAMPLE APPLICATIONS:

(A) 8K ROM, 4K RAM, 2K 'SPARE' RAM

(i) ROM 0,1 (4K) CONNECT CHOSEN PAGE SELECT TO PIN 9 (PS'U')
(ii) ROM 2,3 (4K) —"— 10 (PS'V')
– AND LINK PINS 27-29/26-28
(iii) RAM 0,1,2,3 (4K) CONNECT CHOSEN PAGE SELECT TO PIN 15 (PS'W')
(iv) RAM 4,5 (2K) —"— 35 (PS'X')
– AND LINK PIN 40 (RAM 4) TO CHOSEN 1K BLOCK
– AND LINK PIN 41 (RAM 5) TO ANOTHER 1K BLOCK
(THE POSSIBLE 1K BLOCKS ARE ON PINS 36, 37, 38, 39 – CONNECT ONLY ONE PIN TO EACH RAM SELECT PIN).

(B)

0000 – 07FF	2K ROM (ROM 2)	10-42/26-28	E.G. ZYMON 1
0800 – 0FFF	2K RAM (RAM 4,5)	11-35/38-40/39-41	E.G. ZYMON'S RAM
1000 – 1FFF	1K RAM (RAM 0,1,2,3)	15-43	E.G. BASIC'S RAM
E000 – EFFF	4K ROM (ROM 0,1)	9-20	E.G. BASIC (6K MAX)
F000 – F7FF	2K ROM (ROM 3)	1-19/6-7/29-2	E.G. BASIC (6K MAX)

(C)

8000 – 8FFF	4K RAM (RAM 0,1,2,3)	15-50	E.G. RAM EXPANSION (IF 0000-7FFF IS ALREADY RAM)
9000 – 98FF	2K RAM (RAM 4,5)	35-51/36-40/37-41	E.G. RAM EXPANSION (IF 0000-7FFF IS ALREADY RAM)
E000 – EFFF	4K ROM (ROM 0,1)	9-20	E.G BASIC (8K MAX)
F000 – FFFF	4K ROM (ROM 2,3)	10-19/26-28/27-29	E.G BASIC (8K MAX)

(D)

0000 – 0FFF	4K ROM (ROM 0,1)	9-42	E.G NIBL-MM FIRST 4K
1000 – 1FFF	4K RAM (RAM 0,1,2,3)	15-43	E.G. PAGE 1 NIBL RAM
2000 – 23FF	1K RAM (RAM 4)	7-8/1-44/2-40	E.G PAGE 2 —"—
E000 – E7FF	2K ROM (ROM 2)	10-20/26-28	E.G. KITBUG-MM + NIBL-MM
E800 – EBFF	1K – VACANT –		
EC00 – EFFF	1K RAM (RAM 5)	11-35/39-41	E.G. KITBUG RAM
F000 – F7FF	2K ROM (ROM 3)	(19-29)	E.G. OTHER FIRMWARE (E.G PROM P'GR, TAPE ETC.)

(– LAST ITEM IS ONLY PARTIALLY DECODED – IE. OCCUPIES F000-FFFF)

(E)

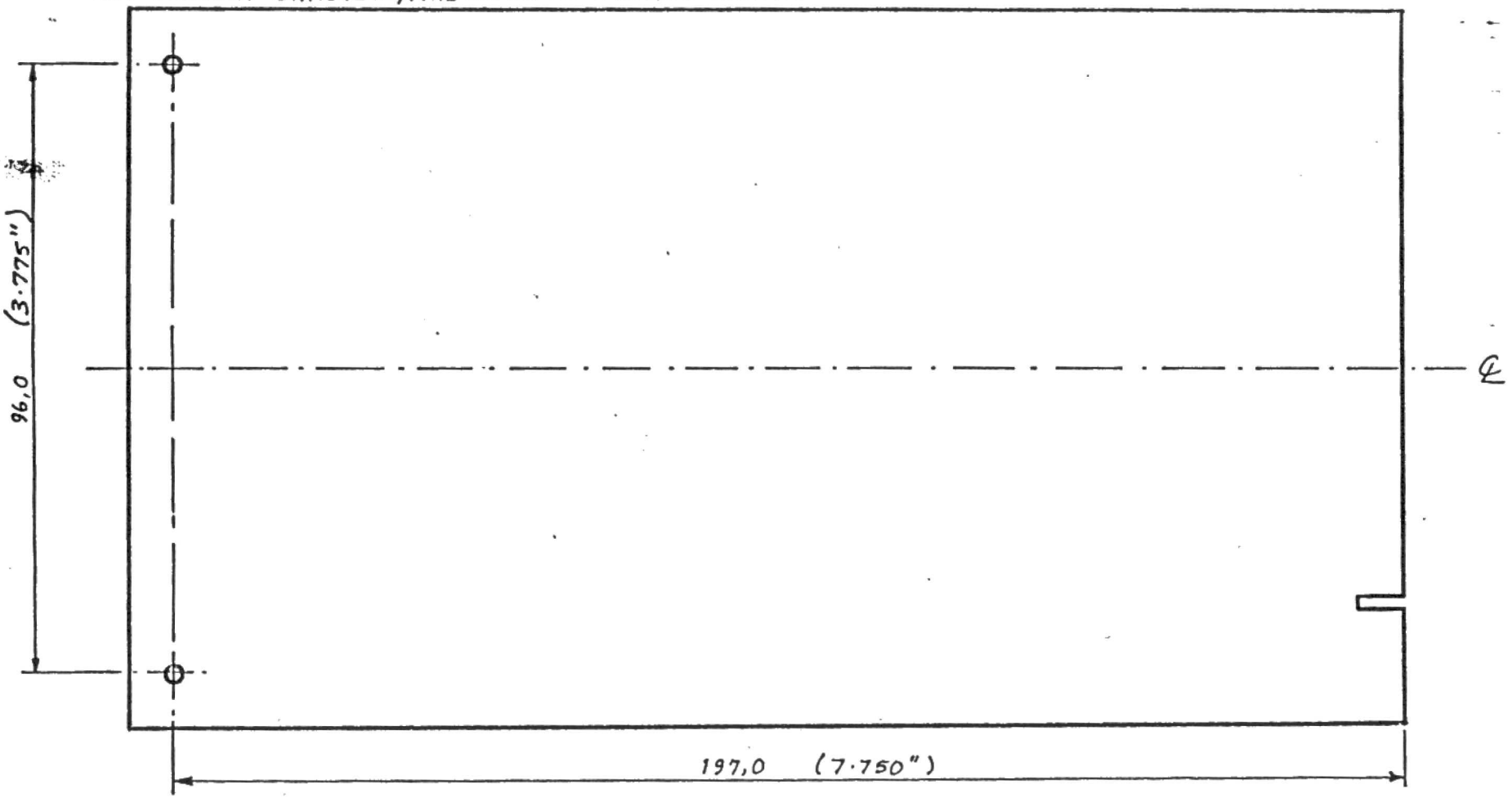
0000 – 0FFF	4K ROM (ROM 0,1)	9-42	E.G. NIBL-MM FIRST 4K
1000 – 1FFF	4K RAM (RAM 0,1,2,3)	15-43	E.G. PAGE1 NIBL RAM
2000 – 27FF	2K ROM (ROM 3)	1-44/6-7/2-29	E.G PAGE2 NIBL "START UP" ROM PROGRAM
E000 – E7FF	2K ROM (ROM 2)	10-20/26-28	E.G. KITBUG-MM + NIBL-MM
E800 – EFFF	2K ROM (RAM 4,5)	11-35/38-40/39-41	E.G. KITBUG RAM

THE BUFFER ON THE DATA BUS IS AUTOMATICALLY ENABLED WHEN THE ABOVE SELECTIONS ARE MADE.

EXPLANATION OF LINK DESCRIPTION
EXAMPLE: 1-2/3-4/5-6 MEANS LINK PIN 1 TO 2, ALSO PIN 3 TO 4, AND PIN 5 TO 6 } THREE LINKS TO BE MADE IN ALL

Drwn	D. M. P	Greenbank Electronics
Date	2-6-81	RRM-14 GENERAL GUIDANCE ON ADDRESS SELECTION LINKS ETC.
Scale	–	

NOTE: MARKINGS FOR HOLE CENTRES
WHICH ARE ON THE CARD DO NOT
SUIT CURRENT BRACKETS, AND SHOULD BE DISREGARDED.



TWO HOLES 3,2 DIA (1/8")

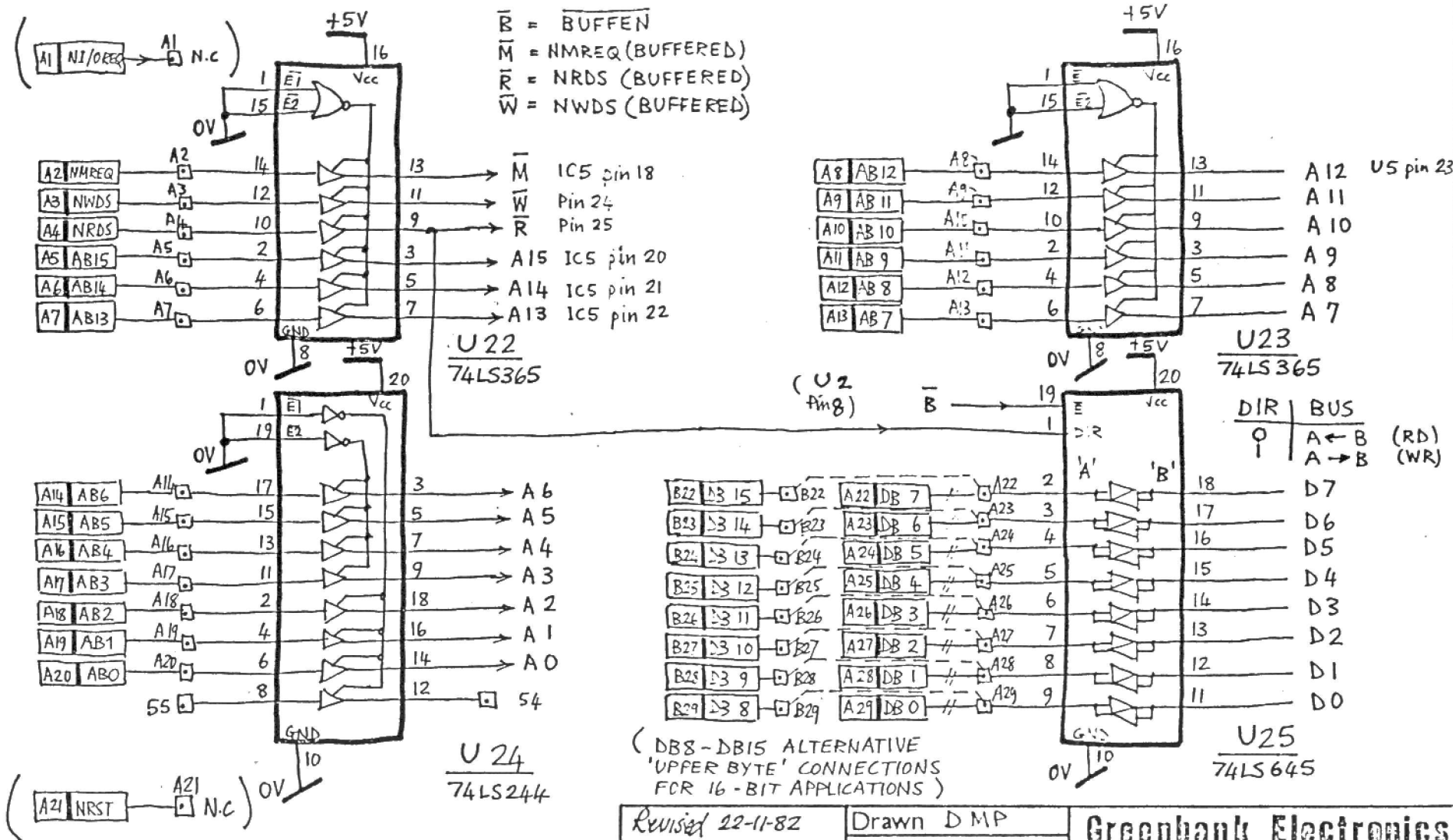
INTERNATIONAL CARD SIZE NOMINAL
DIMENSIONS 203 × 114 (8" × 4½")

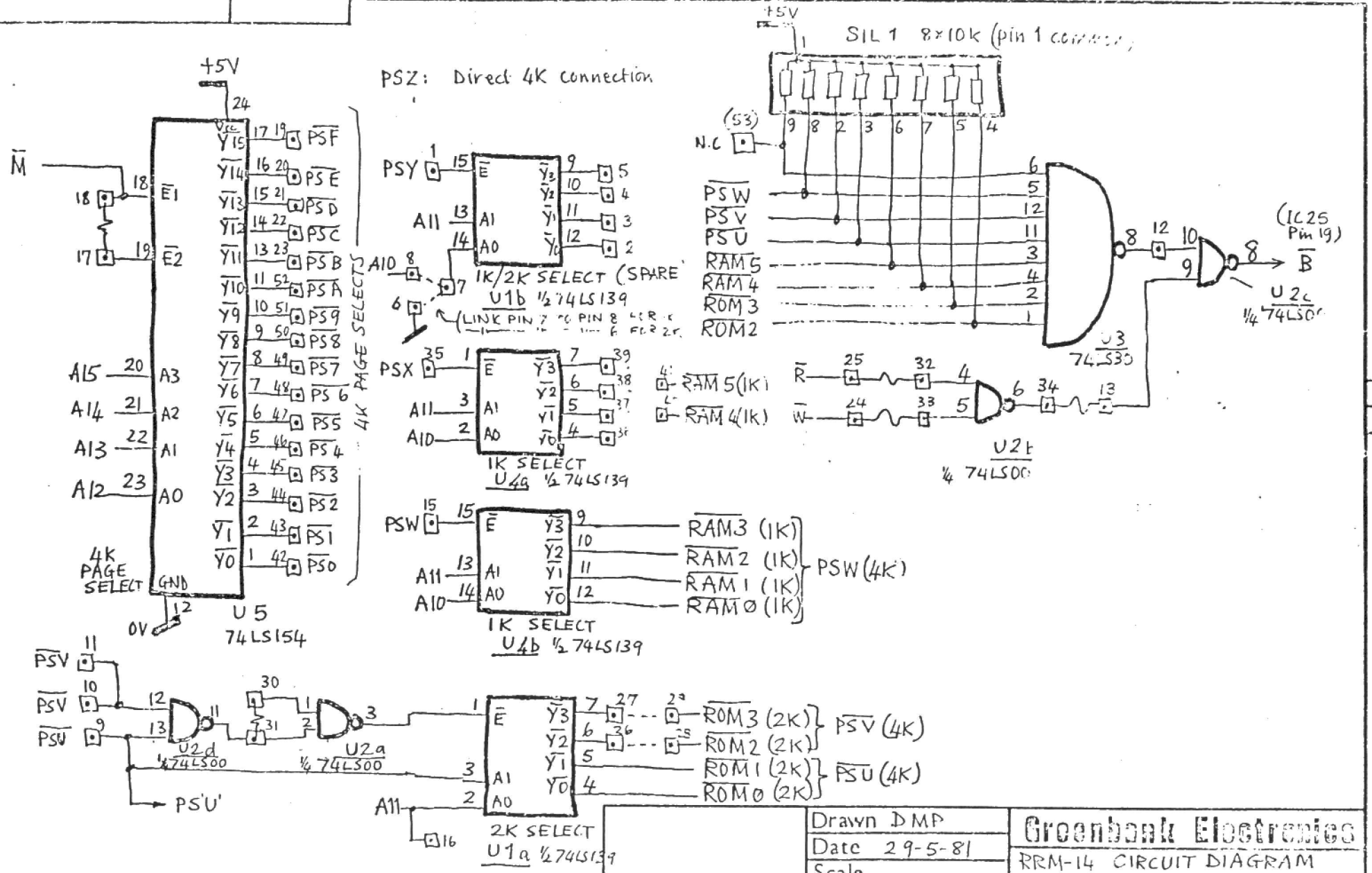
NEW DIMENSIONS
ADDED 22-11-82.

Drawn	D.M.P
Date	27-5-81
Scale	1:1
Dims:	mm

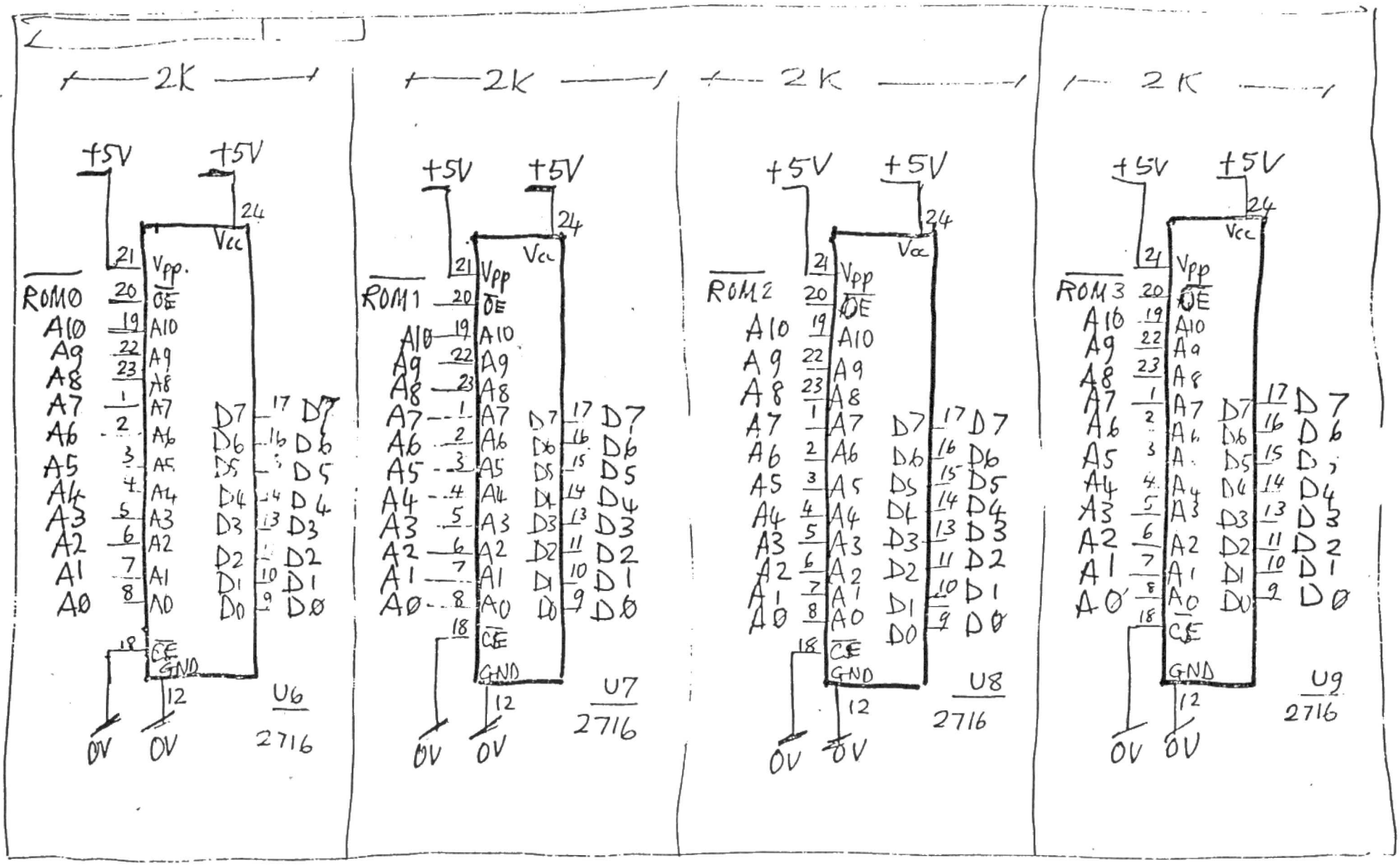
Greenbank Electronics

INTERNATIONAL CARD DRILLING DETAILS FOR CARD FRONT MOUNTING BRACKETS

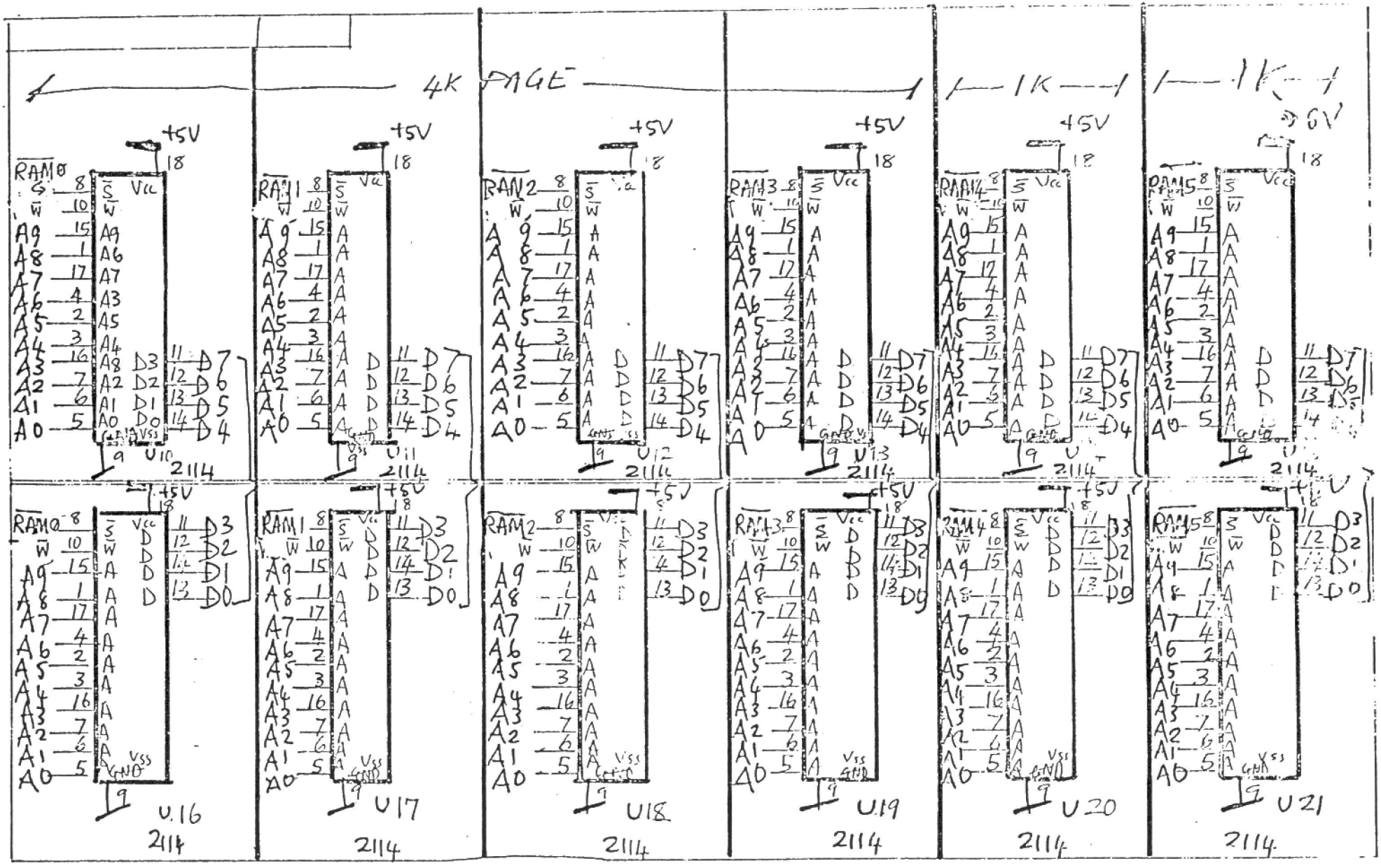

$\overline{B}$ = BUFFEN
$\overline{M}$ = NMREQ (BUFFERED)
$\overline{R}$ = NRDS (BUFFERED)
$\overline{W}$ = NWDS (BUFFERED)
+5V
0V
A1 NI/OREQ → A1 N.C
A2 NMREQ
A3 NWDS
A4 NRDS
A5 AB15
A6 AB14
A7 AB13
$\overline{M}$ IC5 pin 18
$\overline{W}$ Pin 24
$\overline{R}$ Pin 25
A15 IC5 pin 20
A14 IC5 pin 21
A13 IC5 pin 22
U22
74LS365
A8 AB12
A9 AB11
A10 AB10
A11 AB9
A12 AB8
A13 AB7
A12 U5 pin 23
A11
A10
A9
A8
A7
U23
74LS365
(U2 pin8)
$\overline{B}$
DIR
BUS
A ← B (RD)
A → B (WR)
A14 AB6
A15 AB5
A16 AB4
A17 AB3
A18 AB2
A19 AB1
A20 AB0
55
A6
A5
A4
A3
A2
A1
A0
54
U24
74LS244
A21 NRST → A21 N.C
B22 DB15 — A22 DB7
B23 DB14 — A23 DB6
B24 DB13 — A24 DB5
B25 DB12 — A25 DB4
B26 DB11 — A26 DB3
B27 DB10 — A27 DB2
B28 DB9 — A28 DB1
B29 DB8 — A29 DB0
'A' 'B'
D7
D6
D5
D4
D3
D2
D1
D0
U25
74LS645
(DB8-DB15 ALTERNATIVE 'UPPER BYTE' CONNECTIONS FOR 16-BIT APPLICATIONS)
Revised 22-11-82
Drawn DMP
Date 29-5-81
Scale –
Greenbank Electronics
RRM1-14 CIRCUIT DIAGRAM
SHEET 1 ADDR, DATA BUFFERS



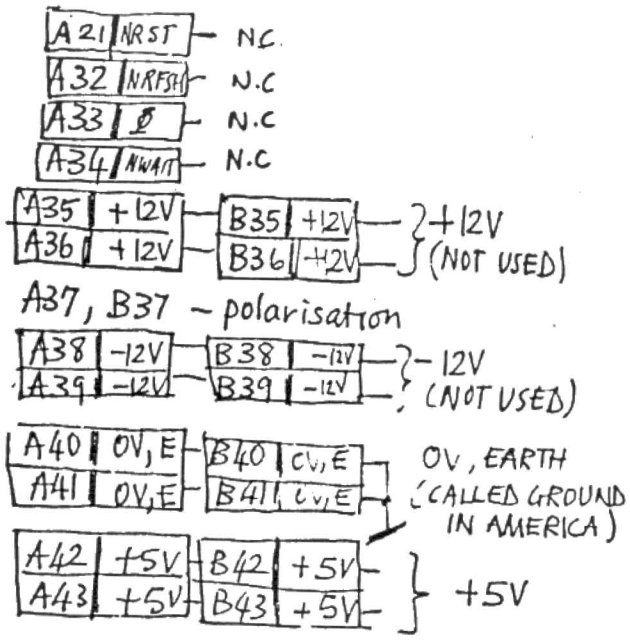
	Drawn DMP	Greenbank Electronics
	Date 29-5-81	RRM-14 CIRCUIT DIAGRAM
	Scale	SHEET 2 ADDRESS SELECTION

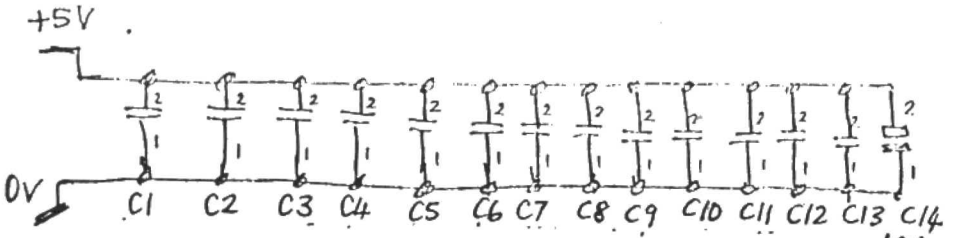


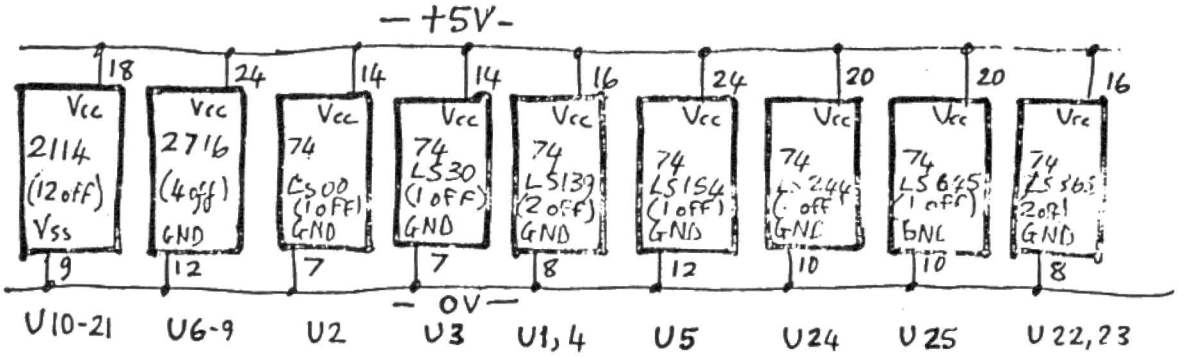
RRM-1 CIRCUIT DIAGRAM
SHEET 3 ROMS



RR-M-14 CIRCUIT DIAGRAM
SHEET 4 RAMs

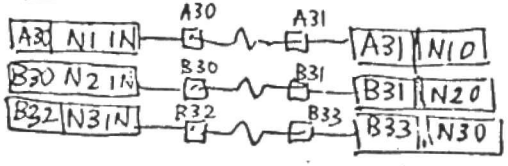






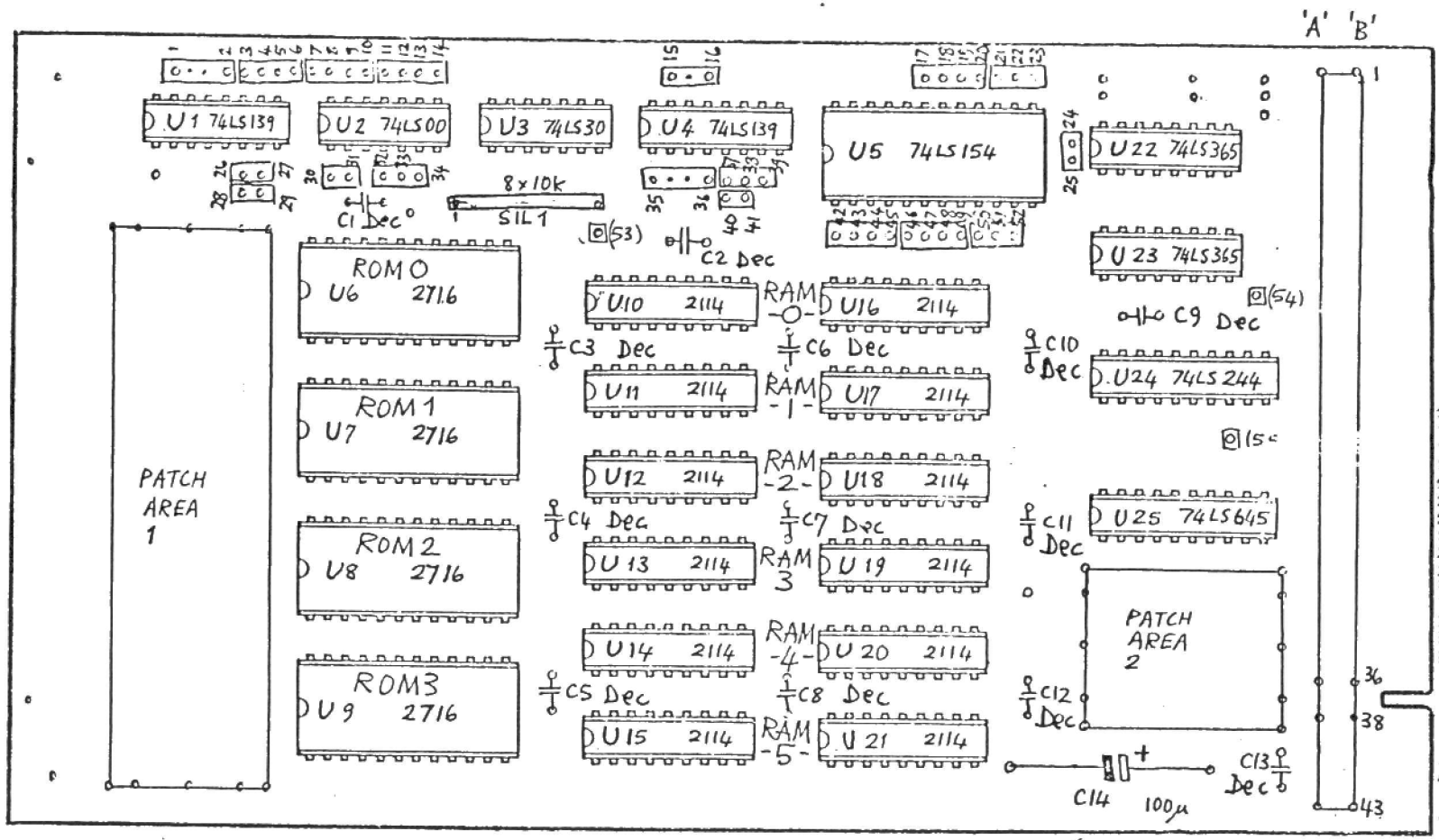
Daisy chain lines (if used)

Link A30, A31
B30, B31
B32, B33



Symbols
- Terminal Pad or connection point.
- Possible route for signal via jumper link
- Usual route for signal via jumper link

RRM-14 CIRCUIT DIAGRAM
SHEET 5 POWER SUPPLIES ETC



'A'	'B'
1A (NI/O REQ)	1B (
2A NMREQ	2B (
3A NWDS	3B (
4A NRDS	4B (
5A AB15	5B (
6A AB14	6B (
7A AB13	7B (
8A AB12	8B (
9A AB11	9B (
10A AB10	10B (
11A AB9	11B (
12A AB8	12B (
13A AB7	13B (AB2
14A AB6	14B (AB2
15A AB5	15B (AB2
16A AB4	16B (AB20
17A AB3	17B (AB19
18A AB2	18B (AB18
19A AB1	19B (AB17
20A AB0	20B (AB16
21A (NRST	21B
22A DB7	22B
23A DB6	23B
24A DB5	24B D
25A DB4	25B D
26A DB3	26B (D
27A DB2	27B (DB 10)
28A DB1	28B (DB 9)
29A DB0	29B (DB 8)
30A (NI IN)	30B (N2 IN
31A (NI OUT)	31B (N2
32A (NRFSII)	32B (N3
33A (ø)	33B (
34A NWAIT	34B (
35A (+12V)	35B (+12
36A (+12V)	36B (+12
37A POLARISING	37B POLARISING
38A (-12V)	38B (-12V)
39A (-12V)	39B (-12V)
40A OV,E	40B OV,E
41A OV,E	41B OV,E
42A +5V	42B +5V
43A +5V	43B +5V

(SIGNALS AND COMPONENTS IN BRACKETS ARE NOT NECESSARILY USED ON THIS BOARD)

Revised 22-11-82	Drawn DMP	Greenbank Electronics
	Date 27-5-81	RRM-14 ASSEMBLY DIAGRAM
	Scale 1:1	

COMPONENT PARTS LIST FOR RRM-4

Issue: 2 Revised 22-11-82 Date: June 1981

LISTED BY COMPONENT REFERENCE NO

Capacitors 47-100n are decoupling grade poly or ceramic

C1	47-100n	0·2"	C8	47-100n	0·2"
C2	47-100n	0·2"	C9	47-100n	0·2"
C3	47-100n	0·2"	C10	47-100n	0·2"
C4	47-100n	0·2"	C11	47-100n	0·2"
C5	47-100n	0·2"	C12	47-100n	0·2"
C6	47-100n	0·2"	C13	47-100n	0·2"
C7	47-100n	0·2"	C14	100µ	1·2"

Integrated Circuits (Use sockets)

U1	74LS139	(U14	2114)
U2	74LS00	(U15	2114)
U3	74LS30	(U16	2114)
U4	74LS139	(U17	2114)
U5	74LS154	(U18	2114)
(U6	2716)	(U19	2114)
(U7	2716)	(U20	2114)
(U8	2716)	(U21	2114)
(U9	2716)	U22	74LS365
(U10	2114)	U23	74LS365
(U11	2114)	U24	74LS244
(U12	2114)	U25	74LS645
(U13	2114)		

(U6–U21 optional)

SIL Resistor Pack (Use 'Solderon' Pins)

SIL1 8×10k Pin 1 common (9-pin)

0·1" Pitch Pin Assemblies

P1,2 1×4-position with centre posts removed
P3-14 3×4-position unmodified
P15,16 1×3-position with centre post removed
P17-20 1×4-position unmodified
P21-23 1×3-position unmodified
P24-31 4×2-position unmodified
P32-34 1×3-position unmodified
P35,36 1×4-position with centre posts removed
P37-39 1×3-position unmodified
P40,41 1×2-position unmodified
P42-49 2×4-position unmodified
P50-52 1×3-position unmodified

Sundry

IC Sockets, other hardware, options see below

LISTED BY COMPONENT VALUE

Capacitors

Dec	13	C1-13	0·2"
100µ	1	C14	1·2"

'Dec' means 47-100nF Decoupling grade poly or ceramic

Integrated Circuits (Use sockets)

(2114)	12	U10-U21	(18 pin)
(2716)	4	U6-U9	(24 ")
74LS00	1	U2	(14 ")
74LS30	1	U3	(14 ")
74LS139	2	U1,4	(16 ")
74LS154	1	U5	(24 ")
74LS365	2	U.22,23	(16 ")
74LS244	1	U24	(20 ")
74LS645	1	U.25	(20 ")

SIL Resistor Pack (Use 'Solderon' Pins)

SIL1 8×10k Pin 1 common (9-pin)

0·1" Pitch Pin Assemblies

2 posn. unmodified	5		P14-31,40,41
3 posn. with centre post removed.	5	1	P15-16
3 posn. unmodified		4	P3-14,32-34
4 posn. with centre posts removed	8	2	P1,2,35,36
4 posn. unmodified		6	P3-14,42-49

Sundry

IC Sockets, other hardware, options see below

DIL Sockets.

14-pin	2	U2,3
16-pin	4	U1,4,22,23
18-pin	12	U10-21
20-pin	2	U24,25
24-pin	5	U5-9

'Solderon Pins'

9-pin 1 SIL 1

Prestripped Wire For interconnecting P1-52, + Spares

10 lengths 38 mm
5 lengths 75 mm
5 lengths 114 mm
5 lengths 178 mm

Optional U6-21 :- these not supplied in kit.
1" Front Panel & mounting brackets.

(KIT INCLUDES ALL ITEMS WHICH ARE NOT OPTIONAL)